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FOR

TARGET CONTROL SYSTEM

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TARGET CONTROL SYSTEM

Technical Field

[0001] The present disclosure relates to devices to control the presentation timing and presentation count for target practice.

Background

[0002] Increasing one's skill at shooting a handgun requires practice. Professional shooting courses provide access to sophisticated rotating target practice systems. Some of these systems are manually controlled by the trainer; others provide computerized controls. To simulate real-world shooting situations, decrease reaction time, and in general improve shooting skills, the instructor will operate and/or configure the target practice system to provide a variety of target presentation times and target presentation counts to the shooter.

[0003] Challenges arise once the shooter has completed the course. The shooter should continue to practice in order to maintain and/or improve shooting skills. Often the most convenient and/or practical places to practice are locations without access to utility-generated power. These locations are often located outdoors, in environmentally rugged conditions (high humidity, dirt and dust, precipitation, rough terrain, etc.). The shooter often practices alone. Portability, simplicity of operation, and durability thus become important considerations in providing a target control system that is to be transported, set up, and operated by a single shooter.

[0004] Experience teaches that practice value may increase when the shooter cannot anticipate the target's action. Target presentation time, delay, and count should thus be made unpredictable to some extent. The target control system should have the capability to expand beyond control of a single target, and should be cost-effective for individuals.

[0005] Target control system are available from a number of providers, including Target Timers, Porta Target, Action Target, Beacon Target, STS Targets, Caswell, and Speedwell. However, a need remains for

a target control system for individual shooters that is rugged, portable, simple to set up and operate, expandable, and that provides unpredictable target delay times, presentation times, and presentation counts.

Summary

[0006] The following summary is intended to highlight and introduce some aspects of the disclosed embodiments, but not to limit the scope of the invention. Thereafter, a detailed description of illustrated embodiments is presented, which will permit one skilled in the relevant art to make and use aspects of the invention. One skilled in the relevant art can obtain a full appreciation of aspects of the invention from the subsequent detailed description, read together with the figures, and from the claims (which follow the detailed description).

[0007] A target controller includes a first counter configured to count at a first rate and a second counter configured to count at a second rate. The first and second counters cooperate to determine a delay between receipt of a start signal and target presentation. A third counter determines a target presentation duration, and a fourth counter determines a target presentation count.

Brief Description of the Drawings

[0008] The headings provided herein are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

[0009] In the drawings, the same reference numbers and acronyms identify elements or acts with the same or similar functionality for ease of understanding and convenience. To easily identify the discussion of any particular element or act, the most significant digit or digits in a reference number refer to the figure number in which that element is first introduced.

[0010] Figure 1 is an illustration of an embodiment of a target control system.

[0011] Figure 2 is a high-level block diagram of an embodiment of a target control circuit.

[0012] Figure 3 is a low-level block diagram of an embodiment of a target control circuit.

[0013] Figure 4 is a block diagram of an embodiment of variable delay generator logic.

[0014] Figure 5 is a block diagram of an embodiment of output pulse control logic.

[0015] Figure 6 is a block diagram of an embodiment of duration control logic.

[0016] Figure 7 is a block diagram of an embodiment of count control logic.

[0017] Figure 8 is a block diagram of an embodiment of start/repeat logic.

[0018] Figure 9 is a flow chart of an embodiment of a process to provide a variable delay before target presentation.

[0019] Figure 10 is a flow chart of an embodiment of a process of providing a selection of pre-selected or unpredictable target presentation time.

[0020] Figures 11 is a flow chart of an embodiment of a process of providing a selection of pre-selected or unpredictable target presentation count.

[0021] Figures 12-15 are timing diagrams of an embodiment of signals involved in providing a target presentation delay and target presentation time.

[0022] Figure 16 is a timing diagram of an embodiment of signals involved in providing a target presentation count.

Detailed Description

[0023] The invention will now be described with respect to various embodiments. The following description provides specific details for a thorough understanding of, and enabling description for, these embodiments of the invention. However, one skilled in the art will understand that the invention may be practiced without these details.

In other instances, well known structures and functions have not been shown or described in detail to avoid unnecessarily obscuring the description of the embodiments of the invention. References to "one embodiment" or "an embodiment" do not necessarily refer to the same embodiment, although they may.

[0024] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "above," "below" and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. When the claims use the word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

[0025] Herein, "logic" refers to any information having the form of instruction signals and/or data that may be applied to affect the operation of a processing device. Examples of processing devices are computer processors (processing units), microprocessors, digital signal processors, controllers and microcontrollers, and so on. Logic may be formed from signals stored in a device memory. Software is one example of such logic. Examples of device memories that may comprise logic include RAM (random access memory), flash memories, ROMS (read-only memories), EPROMS (erasable programmable read-only memories), and EEPROMS. Logic may also be comprised by digital and/or analog hardware circuits, for example, hardware circuits comprising counters, flip-flops, switches, delays, logical AND, OR, XOR, NAND, NOR, and other logical operations. Logic may be formed from combinations of software and hardware.

[0026] Figure 1 is an illustration of an embodiment of a target control system. The target control system 100 comprises a presentation

count control 102, a presentation time control 104, and a start button 106. The presentation count control 102 has a "random" setting 108 to cause an unpredictable number of target presentations. The presentation time control 104 has a "random" setting 110 to cause unpredictable target presentation time.

[0027] Figure 2 is a high-level block diagram of an embodiment of a target control circuit. Variable delay generator logic 202 is coupled to output pulse control logic 204. The variable delay generator logic 202 generates a signal after an unpredictable time interval has elapsed after the shooter activates the start button 106, or after a previous target presentation is complete. The output pulse control logic 204 provides a signal to cause the presentation of the target to the shooter. The output pulse control logic 204 is coupled to duration control logic 206 and count control logic 208. The duration control logic 206 determines the time interval that the target is presented to the shooter. This time interval may be an interval determined by the setting of the presentation time control 104, or an unpredictable time interval when the presentation control is set to the random setting 110. The count control logic 208 determines the number of times that the target is presented to the shooter. This count may be a number determined by the setting of the presentation count control 102, or may be an unpredictable number when the presentation count control 102 is set to the random setting 108. The duration control logic 206 is coupled to the output pulse control logic 204 and to start/repeat logic 210. The start/repeat logic 210 creates signals to start the target presentation after the shooter presses the start button 106, and to repeat target presentation if the control settings so determine. The count control logic 208 is coupled to the start/repeat logic 210, and the start/repeat logic 210 is coupled to output pulse control logic 204.

[0028] Figure 3 is a low-level block diagram of an embodiment of a target control circuit. Functional blocks within this overall circuit are described in conjunction with Figures 4-8. A clock 302 is coupled to a counter 304 and a clock divider 306. The counter 304 is coupled to another counter 308. The counter 304 is utilized to provide

unpredictable presentation time and count behavior, in a manner more fully described in conjunction with Figures 4-8. The counter 304 is coupled to switch 322 and switch 330. The clock divider 306 is coupled to the counter 308 and to a counter 320. A delay 310 is coupled to the counter 308 and to a flip-flop (FF) 314. The clock 302, counters 304, 308, divider 306, and delay 310 comprise an embodiment of variable delay generator logic 202 and are more fully described in conjunction with Figure 4.

[0029] The counter 308 is coupled to a nor gate 312. The nor gate 312 is coupled to a FF 318. The FF 314 is coupled to the nor gate 312 and a counter 320. A nor gate 316 is coupled to the FF 318. The FF 318 is coupled to the counter 320, the FF 314, and a counter 328. The nor gates 312, 316 and FFs 314, 318 comprise an embodiment of output pulse control logic 204 and are more fully described in conjunction with Figure 5.

[0030] The counter 320 is coupled to the nor gate 316 and a nor gate 336. A switch 322 is coupled to the counter 320. A coder 324 is coupled to the switch 322, and an analog switch 326 (such as the presentation time control 104) is coupled to the coder 324. The counter 320, coder 324, switch 322, and analog switch 326 comprise an embodiment of duration control logic 206 that is more fully described in conjunction with Figure 6.

[0031] A counter 328 is coupled to the nor gate 336. A switch 330 is coupled to the counter 328. A coder 332 is coupled to the switch 330, and an analog switch 334 is coupled to the coder 332. The counter 328, switch 330, coder 332, and analog switch 334 comprise an embodiment of presentation count control logic 208 that is more fully described in conjunction with Figure 7.

[0032] The nor gate 336 is coupled to a nor gate 338. The nor gate 338 is coupled to the delay 310. A momentary contact button 340 (such as the start button 106) is coupled to the nor gate 338. The momentary contact button 340 is coupled to the counter 328. The momentary contact button 340 and nor gates 336, 338 comprise an embodiment

of start/repeat logic 210 that is more fully described in conjunction with Figure 8.

[0033] Figure 4 is a block diagram of an embodiment of variable delay generator logic 202. The clock 302 produces a clock signal cp302 that is applied to the count input of the counter 304. The clock signal cp302 is also applied to the divider 306. The divider produces a lower-frequency clock signal cp306 (for example, by producing a signal for every seven times cp302 is applied). The signal cp306 is applied to the count input of counter 308. The delay 310 receives a start signal from the start/repeat logic and asserts a signal o310 for a predetermined interval after receipt of the start signal. The signal o310 disables the count enable of counter 308, while enabling the load value input of the counter 308. When the load value input is enabled, the count value of counter 304 is loaded via output count304 to the counter 308 as an initial count value and latched when the load value input goes low. The counter 308 then begins counting up from the loaded initial value (which varies unpredictably based upon when the start signal was received) according to the frequency of signal cp306. Once the counter 308 reaches its count limit, it produces an output signal tc308.

[0034] Figure 5 is a block diagram of an embodiment of output pulse control logic. The set input of the FF 314 receives the signal o310 from the delay 310. The FF 314 has outputs Q and –Q (Q bar) to provide signals q314 and –q314, respectively. The signal -q314 is applied to an input of the nor gate 312. The other input of the nor gate 312 is coupled to receive the signal tc308. The output signal o312 of the nor gate 312 is applied to the set input of the FF 318. The output signal of the nor gate 316 is applied to the reset input of the FF 318. The FF 318 has Q and –Q outputs to provide signals q318 and –q318, respectively.

[0035] Figure 6 is a block diagram of an embodiment of duration control logic. The switch 322 receives the count value count304 from the counter 304. The switch 322 receives a coded value of a preset presentation time selection from the coder 324. The coder receives

the preset time setting from the analog switch 326, which comprises a set of selectable fixed values for the presentation duration, and encodes the setting. For example, the analog switch 326 may assert a signal on one of eight outputs, depending on the setting, and the coder 324 may form a three bit value to represent the output of the analog switch 326. A signal from the analog switch 326 is applied to the select input sel322 of the switch 322, to cause the switch 322 to select either the time value provided from the coder 324, or the value of signal count304. The value selected by the switch 322 is provided to the counter 320. The counter 320 loads this value as an initial count value when the q314 signal applied at input load320 is asserted and latched when the signal applied at load320 goes low. The signal –q318 is applied to the count enable input ce320 of the counter 320. The signal cp306 is applied to the count input of the counter 320. When –q318 is low, the count of counter 320 increments at a rate determined by the frequency of cp306. When the counter 320 reaches its count limit, it outputs a signal tc320.

[0036] Figure 7 is a block diagram of an embodiment of count control logic 208. The switch 330 receives the count value count304 from the counter 304. The switch 330 receives a coded value of a preset presentation count selection from the coder 332. The coder receives the preset count setting from the analog switch 334, which comprises a set of selectable fixed values for the presentation count, and encodes the setting. For example, the analog switch 334 may assert a signal on one of eight outputs, depending on the setting, and the coder 332 may form a three bit value to represent the output of the analog switch 334. A signal from the analog switch 334 is applied to the select input sel330 of the switch 330, to cause the switch 330 to select either the count value provided from the coder 332, or the value of signal count304. The value selected by the switch 330 is provided to the counter 328. The counter 328 loads this value as a count target value when a signal is asserted at input load328, and latches the value when load328 goes low. The output q3_328 is applied to the count enable input ce328 of the counter 328. The signal

q318 is applied to the count input cp328 of the counter 328. The count of counter 328 increments each time q318 is asserted, e.g. each time there is a target presentation. When the counter 328 reaches its count target, it asserts a signal at q3_328.

[0037] An arrangement similar to that shown in Figures 6 and 7 may be provided to select from a set of selectable fixed times for the interval between when the start signal is received by the delay 310 and when the signal tc308 is produced to cause target presentation. For example, the initial count value loaded to the counter 308 may be selected using a switch coupled through a coder to an analog switch, as either the value of count304 or a value corresponding to the setting of the analog switch.

[0038] Figure 8 is a block diagram of an embodiment of start/repeat logic 210 to repeatedly generate the start signal according to the presentation count determined by the count control logic. The signals q3_328 and tc320 are applied to the inputs of the nor gate 336. The output signal o336 of the nor gate 336 is applied along with the output of the momentary contact button 340 to the inputs of the nor gate 338. When the momentary contact button 340 is pressed, a high signal VCC is applied to an input of the nor gate 338, forcing the output signal o338 (start signal – see Figure 4) low.

[0039] Figure 9 is a flow chart of an embodiment of a process to provide a variable delay before target presentation. At 905 a first clock signal is applied to a first counter. At 910 a second clock signal of different frequency than the first clock signal is applied to a second counter. At 915 a start signal is received. At 920 the start signal causes the second counter to load an initial count from the first counter. At 925 second counter counts up beginning from the loaded initial count. At 930 the second counter generates a signal upon reaching its count limit value. At 935 the signal from the second counter causes target presentation. At 940 the target presentation starts a third counter 940, and at 945 the process concludes.

[0040] Figure 10 is a flow chart of an embodiment of a process of providing a selection of pre-selected or unpredictable target

presentation time. If at 1005 the "random" setting for presentation time has not been selected, the third counter (see Figure 9) loads an initial count from a fixed setting at 1010. If at 1005 the "random" setting for presentation time has been selected, the third counter loads the initial count from the first counter at 1015. At 1020 the third counter generates a signal upon reaching its count limit value. At 1025 this signal ends target presentation, and at 1030 the process concludes.

[0041] Figures 11 is a flow chart of an embodiment of a process of providing a selection of pre-selected or unpredictable target presentation count. If at 1105 the "random" setting for presentation count has not been selected, a fourth counter loads an initial count from a fixed setting at 1110. If at 1105 the "random" setting for presentation count has been selected, the fourth counter loads an initial count from first counter at 1115. At 1120 the fourth counter generates a signal upon reaching its count limit value. At 1125 this signal ends target presentation count, and at 1130 the process concludes.

[0042] Figures 12-15 are timing diagrams of an embodiment of signals involved in providing a target presentation delay and target presentation time.

[0043] In Figure 12, target presentation is initiated by a start signal produced by operation of the start button 106 or by other means. At t0 the start signal transitions low. At t1 the delay output o310 transitions high and remains high for a predetermined delay interval I0. At t3 o310 transitions low. The high-going pulse produced by the delay 310 may be of similar or dissimilar width from the start pulse, but is typically dissimilar. At t4, after a variable delay period I1 determined by the initial count loaded into counter 308, the clock frequency applied to 308, and possibly other factors, the counter 308 reaches its count limit value and tc308 transitions low.

[0044] In Figure 13 the asserted signal o310 is applied to the set input of FF 314 at t5, causing –q314 to transition low at t6 (after a short delay inherent in the FF 314). At t7 tc308 also transitions low as

counter 308 reaches its count limit value. Both inputs to nor gate 312 are now low, and thus at t8 the output signal o312 of the nor gate 312 transitions high. At t9 tc308 transitions high, forcing o312 to transition low at t10.

[0045] In Figure 14, the assertion of o310 (the output of delay 310) causes q314 (the Q output of FF 314) to transition high at t11. At t12 the output o312 of the nor gate 312 transitions high as counter 308 reaches its count limit value. This causes the Q output q318 of FF 318 to transition high at t13, and –q318 to transition low, and results in target presentation to the shooter. Signal q318 is applied to reset FF 314, so that q314 transitions low at t14.

[0046] In Figure 15, at t15 the counter 320 reaches its count limit value and tc320 transitions low. Signal tc320 is applied to both inputs of nor gate 316, so that at t16 the output o316 of nor gate 316 transitions high. The signal o316 is applied to reset the FF 318, so that at t17 - q318 transitions high and q318 transitions low.

[0047] Figure 16 is a timing diagram of an embodiment of signals involved in providing a target presentation count. A target presentation is made during the time that q318 is high. At t20 the target presentation counter 320 reaches its count limit value, a value that may be loaded either from the switch 334 selection, or from the count value count304 of counter 304 (for unpredictable presentation counts). At t20 tc320 transitions low, q318 transitions low (ending the target presentation), and the output o336 of nor gate 336 transitions high because both inputs tc320 and q3_328 are low. This causes the start signal to transition low for the time that tc320 (and hence 0336) are low, e.g. another start pulse is created. This process is repeated at t21 when the second target presentation completes. Each time the target presentation completes, the count of counter 328 is incremented, until at t22 the counter 328 reaches its preset count value, and q3_328 transitions high. At t23 the presentation time counter 320 once again reaches its limit count, and tc320 transitions low. However, this time q3_328 is high, so that o336 is not asserted,

and no start pulse is produced. Thus, target presentation concludes after three presentations.